IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 12, Issue 3 Ver. V (May-June. 2017), PP 79-84
www.iosrjournals.org

A Step-Up 13 Level Inverter with Reduced Switches using PWM Techniques

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Abstract —*In this article, a 13-level single phase cascaded hybrid multilevel inverter with a minimal number of live switches is introduced. In this concept, a switched capacitor (SC) system is intended. The number of output levels is determined by the number of switched capacitor cells. This circuit's design is fairly straightforward, and it is simple to advance it. The gate drive circuits are simplified when the number of live switches is reduced, and power losses are analysed. Using MATLAB/SIMULINK, a 13-level single phase cascaded hybrid multilevel inverter model is created, along with targeted modulation schemes. A single phase induction is driven when this multilevel inverter has been evaluated.*
Index Term/s -- *Induction Motor, Multilevel Inverter, Cascaded H-Bridge, switched capacitor, PWM signal modulated technique.*

I. Introduction

The development of multilevel inverters is essential due to the increasing higher power quality requirements for common industrial applications, residential use, and renewable energy sources including wind, solar, and fuel cells. The standard three level inverters struggle to achieve these requirements of a clean, fresh sinusoidal waveform and a minimal distortion factor. This prompts the introduction of a multilayer inverter as a substitute in situations requiring improved power quality. The multilayer inverters as an alternate solution have attracted a lot of attention for quite a few clever features, such as waveform of output voltage close to sinusoidal voltage and decreased dv/dt stress [1]-[2].

Certainly, there are three different types of multilevel inverter topologies: neutral-point-clamped inverters, flying capacitors, and the H-bridge cascade. These inverters have a good track record for better motor drives and higher power quality in many industrial applications because of their strong performance. Their shortcomings, such as the need for numerous independent voltage sources and the H-bridge cascade structure, are also apparent. Additionally, both capacitor-clamped and neutral-point clamped inverters exhibit the voltage balance issue.

There are now a number of novel multilevel inverter topologies that cannot be classified up to the level of the conventional three classes above, as described in [2] and [3]-[9]. Although a straightforward topology is recommended, multiple dc input voltage is still required. The multilevel inverter coupled inductor approaches were developed in [2] and [5]. Although the arrangements are inadequate, it is challenging to create new, higher level applications [6], [8,] and [9]. Innovative topologies that were generated from switched capacitors (SC) [10] were introduced, but their output voltage values were constrained. Although the multilevel topology described in [7] can be expanded to higher levels, using a large number of live switches increases the cost and quantity of gate equipment requirements.

An innovative multilevel inverter topology bounding a multilevel dc-dc converter and a full bridge is obtained in this work. In the suggested topology only one dc voltage source is required and problems like voltage balancing, huge live switches and difficult gate driver circuits were overcome. The dc-dc conversion is the important key point of whole configuration, which is designed by joining multilevel SC cells. Each SC cells contains a capacitor, an active switch and two diodes. Accordingly the output voltage levels of the suggested inverter could be raised by raising numbers of SC cells.

II. Dc–Dc Multilevel Converter Circuit Description

Fig.1 shows a multilevel inverter which is connected back to back by a dc-dc multilevel converter and a full bridge.

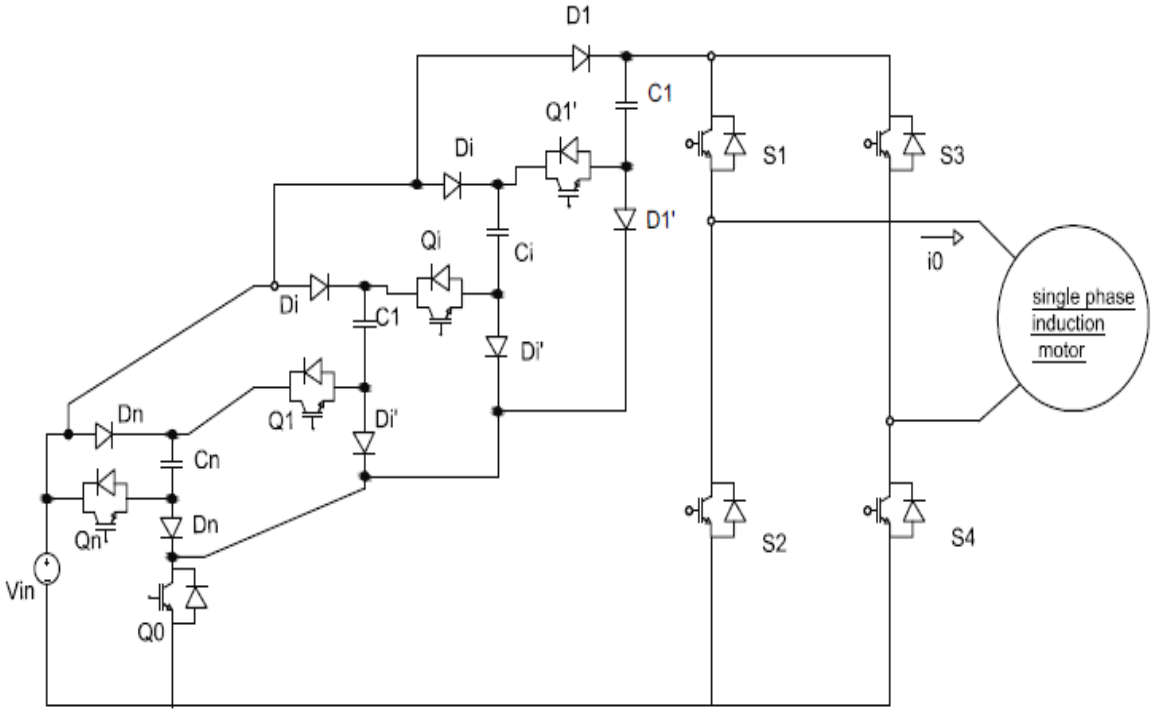

Fig.1 Suggested multilevel inverter

The dc-dc converter part contains number of SC cells which is able to offer the number of n+1 levels of output voltage with respect to different switching states. i.e., 0, + Vin , + 2Vin …… + (n+1) Vin. The following statements are made for analysis

1. The values of all SCs and C_i are sufficient enough and voltage ripple across them are insignificant.
2. All the switching devices are ideal i.e., no voltage drops across any switch.
3. Source power is constant.

A. Zero output level

All SCs and C_i are charged by V_{in} through D_i and D_i' when the switch Q_0 is switched ON while Q_i [i=1,2,….,n] is off. The device S1 is switched ON only for H-bridge, whereas other are off. No voltage is developed for load and the output voltage is consequently equal to zero. The output current i_0 is freewheeling through device S1 and bypass diode of S3 when load does not a pure resistive.

B. $\pm$ V_{in} output level

In this level the operation of converter is similar to that of zero level abovementioned i.e., S_1 and S_4 keeps ON-state while other switches are off. The capacitor voltage is same as input voltage V_{in} i.e., V_{Ci}= V_{in}(i=1,2,….n)Voltage V_{in} is produced by the input is applied straightly to the load, likely the level of - V_{in} can be developed by switching ON of devices S_2 and S_3 whereas S_1 and S_4 are off.

C. $\pm$ i X V_{in} output level

When the device Q_0 is turned off, voltage level i X V_{in} can be developed in dc-dc conversion part by switching ON devices Q_1-Q_{i-1}(i=1,2,....,n) whereas Q_i-Q_n off. In this case, capacitors C_1-$C_{i-1}$are connected in series with inputV_{in} and the net voltage now is i.e. V_{in}+V_{C1}+…..+V_{Ci-1} is developed which is equal to i X V_{in}. This voltage can be made to appear across the load by switching on S_1 and S_4 while S_2 and S_3 are kept off of the full bridge section. Similarly – i X V_{in} is applied across the load, operating in a reverse approach and when i=n the output level is equal to $\pm$n V_{in}.

D. $\pm$(n+1) V_{in} output level

In dc-dc part all capacitors C_i are connected in series with input V_{in} to produce peak voltage level (n+1)when switches Q_1-Q_n are all switches on whereas Q_0 keeps the off state, $\pm$(n+1) can be produced by switching on S_1 and S_4 or S_2 and S_3.

III. Block Diagram Of Multilevel Inverter

As shown in Fig. 2 The source power to the multilevel inverter is provided by DC voltage sources. The multilevel inverter is controlled by PIC micro controller through driver circuit. The power supply to the driver circuit and PIC micro controller is obtained from power supply unit. The single phase induction motor is operated by multilevel inverter. The conduction of switches in the converter are interchanged in order to control the flow of power from input to load and the average value is controlled by modulating the width of the pulses. A trendy method in industrial applications is carrier-based sinusoidal Pulse Width Modulation(SPWM). In SPWM shifting method is used to lower the harmonics in load voltage. The another alternative method is SVM strategy which is used in three level inverters. Methods with low switching frequencies usually achieve one or two commutations of switches throughout one cycle of output voltages, producing a stair case waveform.

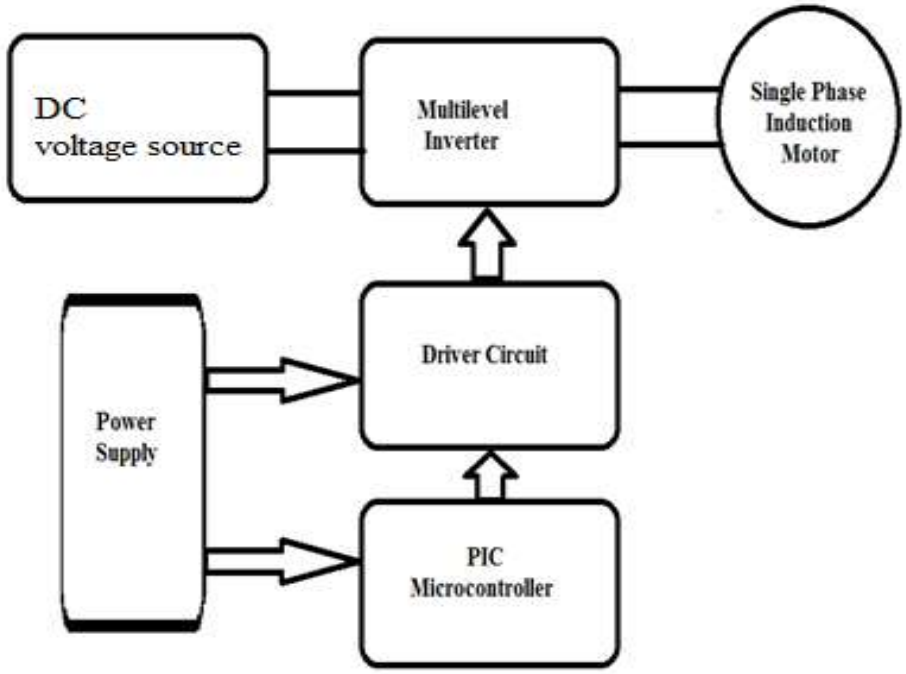

Fig.2 Block Diagram of Multilevel Inverter with single phase induction motor.

IV. Pulse Width Modulation (Pwm)

In the proposed CSI topology, a level based multicarrier PWM strategy implemented for firing the gate terminals of the MOSFET to obtain the current waveform of multilevel inverter.

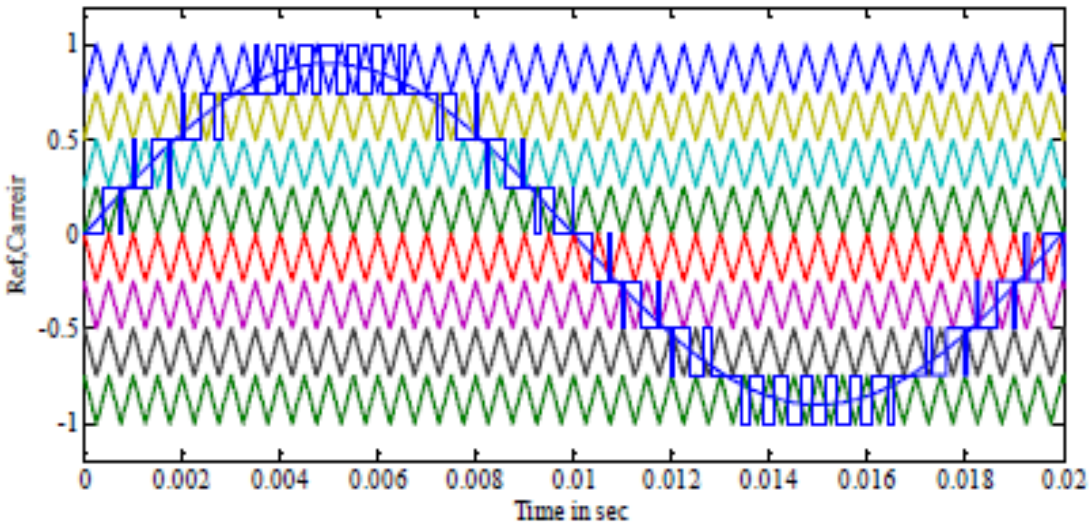

Fig.3. Gate pulse generation

Multicarrier PWM strategy is a comparison of a reference waveform, with vertically shifted carrier signals. In multicarrier PWM technique, m-1 triangular carriers are used for m-level inverter output voltage or current. In this proposed nine-level topology, eight triangular carriers are preferred. In Phase Opposition Disposition (POD), the carriers above the sinusoidal reference zero points are 180 out of phase with those below the zero point. Fig.6 shows the gate pulse generation of proposed CSI with POD strategy with sine reference of modulation index ma = 0.9 and the carrier frequency of 2 kHz.The carrier waveforms have same amplitude Ac and frequency fc. Similarly, the reference waveforms have frequency fref and an amplitude Aref. At every instant, the response of the comparator is decoded to generate the correct switching sequences with respect to the output of the inverter.

V. Simulation Results

The simulink circuit of DC-DC Multilevel converter shown in Fig 4. Fig.5 and Fig. 6 shows the AC output voltage and DC output current of DC-DC multilevel converter. The Total Harmonic Distortions (THD) for single phase inverter is shown in Fig 7.

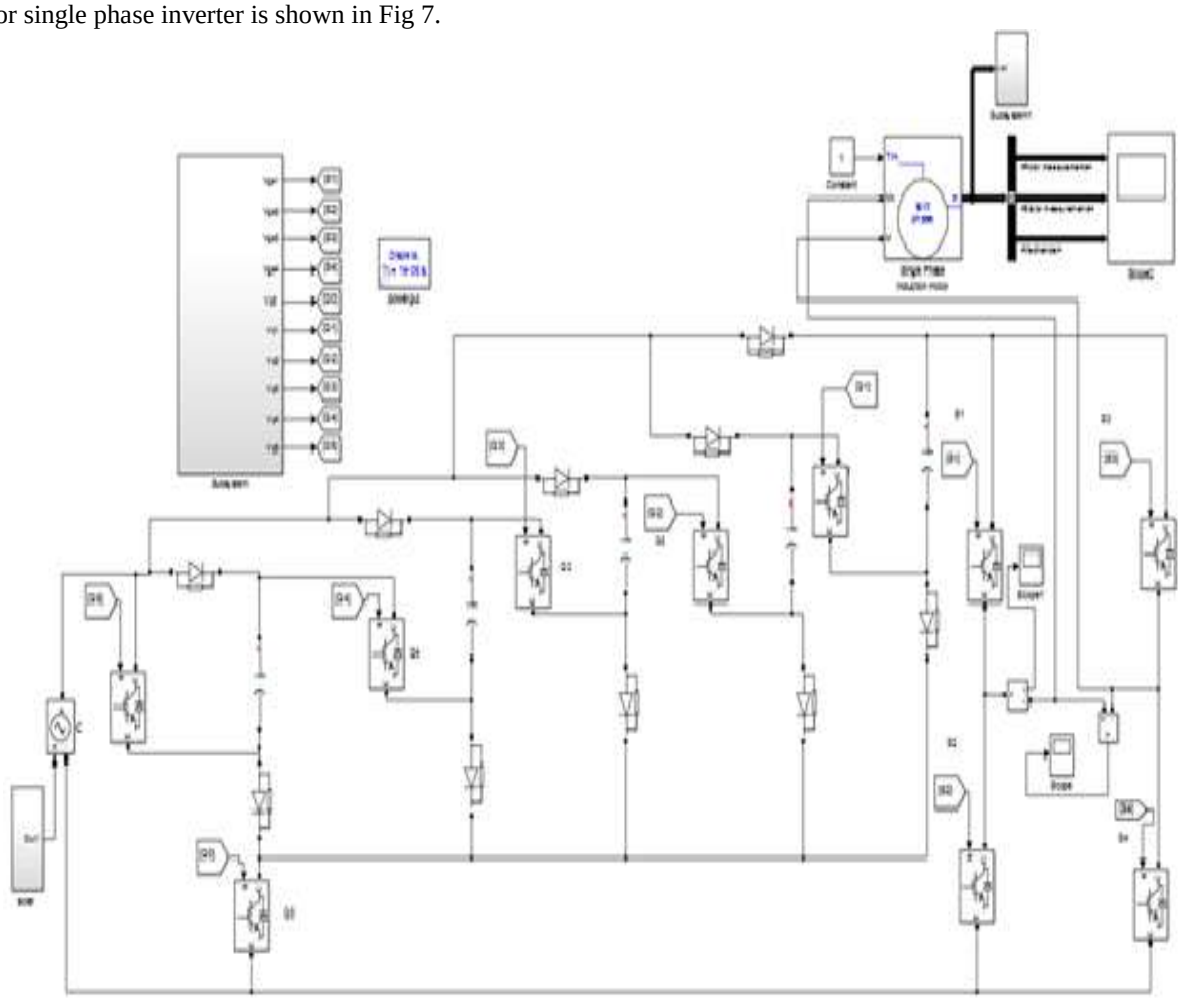

Fig.4 Simulation of Multilevel inverter

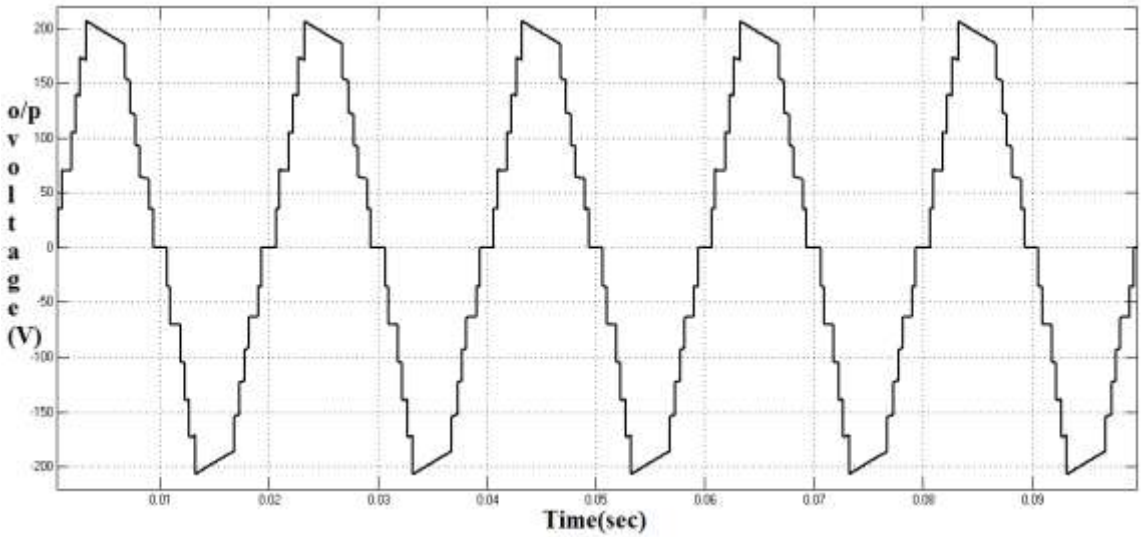

Fig.5Waveform of Output Voltage of Multilevel Inverter

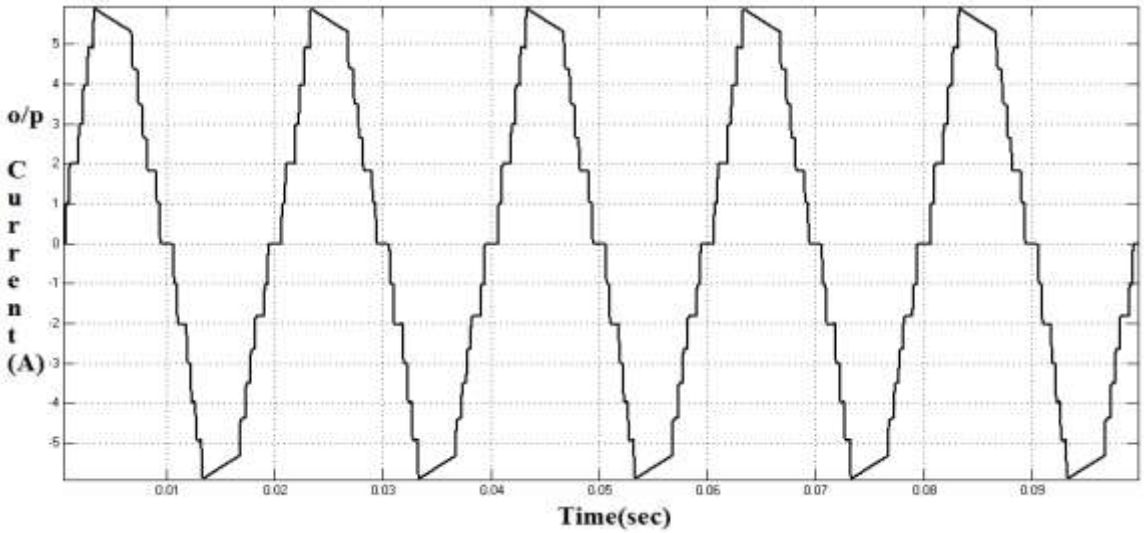

Fig.6Waveform of Output Current of Multilevel Inverter

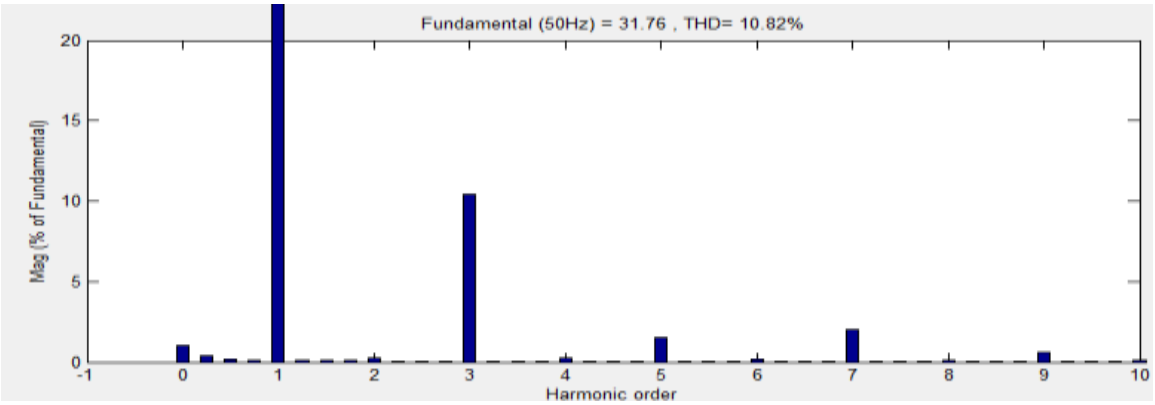

Fig.7 Waveform of Total Harmonic Distortion.

S.NO	PARAMETER	VALUES
1	DC Input voltage (V_{dc})	36V
2	DC – DC Multilevel converter output voltage (V_{dco})	205V
3	Output voltage of Three phase inverter (V_{aco})	205V
4	Total Harmonic Distortions (THD)	10.82%

Table- 1 Input and Output parameter for Multilevel Inverter Model

VI. Conclusion

In this paper, a new Thirteen-level inverter fed induction motor drive is implemented in which SPWM controller is used as it has less complexity than other topologies. The THD is reduced to 10.82 percent whereas 14.20 percent in eleven level(existing) The simulation results of proposed topology of Thirteen level inverter fed induction motor drive are verified using MATLAB. Finally, the operation and performance of the proposed inverter are verified with experiments on an 13-level inverter prototype.

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